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# A REVIEW OF THE FOUNDATION TECHNOLOGIES OF NANO-ELECTRONICS

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**Abstract:** *In this paper we discuss the foundation technologies that have kindled and are reinforcing the shift of microelectronics to nanoelectronics. Nano electronics is the science which deals with the electronic components manufactured and engineered at a molecular scale. Today's electronics world is dominated by the micro-level silicon based technology which follows the famous Moore's law. Further miniaturization is hindered by certain physical, thermal and manufacturing problems. The paper discusses about combating these problems with various nano materials, new device architectures and using them onto the CMOS circuitry. Carbon nanotube (CNT), graphene Nano ribbon (GNR), Semiconducting Nanowire (S-NW) and molecular electronic devices are the potential materials which can modify the pre-existing silicon based technology. Miniaturization of FETs to the nano-level is accompanied by leakage current and power losses, fully depleted tri-gate transistors provide a promising solution. Studies have proved that electrical, thermal, mechanical, physical and chemical properties of nano-materials are superior to silicon. Graphene shows excellent electrical and thermal properties, major research being pursued to exploit these properties by employing graphene in electronics world. This nano-circuitry can find its use in digital circuits, display applications, TFTs, printed electronics, high precision sensors, radio frequency (RF) signal processing and flexible electronics. The paper also discusses various limitations in manufacturing of these nanomaterials at a large scale to launch them in the commercial market. There are certain demerits of the aforementioned nano-materials which stand as challenges to be tackled. The major obstacles are fabrication of such nano-sized FETs, nano-wires and placing them onto the CMOS circuitry with ultra-high precision, high values of yield and a production rate so as to meet the unprecedented demand of these components in the market.*

***Keywords****: Moore's law, Graphene, CNT, MOSFET, Tri-gate transistor.*

## INTRODUCTION

In this paper the foundation technologies leading to the era of Nano electronics is discussed. The extensive industrial development done in the field of electronics is majorly based on silicon based technology which works at the micro scale. The scaling down of size of silicon based technology with time is governed by the famous Moore's law. Today's silicon based electronics has reached the maximum limits of miniaturization in size. Going to the Nano-scale with silicon and the pre-existing technology today pose various physical problems and increment in power losses in the circuit. This hurdle has kindled extensive research in two directions. One direction is the modification of the pre-existing physical structure of FET and MOSFET. Some of the modifications include single-gate fully depleted-substrate transistor (DST), double-gate FINFET and the fully-depleted tri-gate transistor. The other direction of research is to replace the silicon based materials by Nano-materials which show superior electrical, thermal and mechanical properties. Potential candidates to replace silicon are Carbon nanotube (CNT), graphene Nano ribbon (GNR), Semiconducting Nanowire (S-NW) and molecular electronic devices. Combining the above two technologies paves the way to a novel solution. Use of Nano-materials to manufacture the structurally modified transistors maximizes the potential of further reducing the size of electronic circuits.

### 1. MOSFET Basics

The metal oxide semiconductor field-effect transistor (MOSFET) has been the fundamental element and most basic building block for most of the electronic and computing devices. It is widely used a basic on of switch in the realm of digital circuits. A schematic representation of the MOSFET shown in Fig. 1, it shows four terminals viz. source, drain, gate and bulk. The drain and source are the two ends of the switch. The switch can be turned on and off bycontrolling the gate voltage ($V_g$),it controls the conduction of charge carriers throw the channel. The gate has thin oxide thin film coating which insulates it from the channel region. The MOSFETs can be classified into two categories, nMOS and pMOS. The criterion for classification is based on which element is used to dope the silicon used in the MOSFET. A pMOS transistor has heavily doped source and drain by a p-type material such as Boron. The channel is lightly doped with an n-type material such as Phosphorous. Similarly an nMOS transistor has a heavily n-type doped source and drain and lightly p-type doped channel.

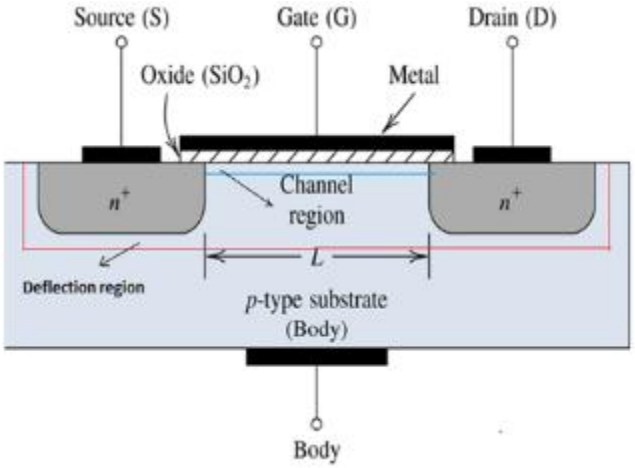


*Fig. 1. Schematic representation of a general MOSFET*

When a pMOS transistor is in OFF state due to the interaction of holes and electrons near the highly p-type doped source and drain, a depletion layer is formed which is void of any charge carriers. Thus, there wouldn't be any current in the channel. As the gate voltage keeps on decreasing the electrons are pushed away from the depletion region to get a continuous band of p-type material from the source to the drain. An electric field is set up across the source and drain, which facilitates the flow of electrons and a current is set up from the source to drain.

MOSFETs are essentially used to make logic gates such as NAND, AND, OR gates. Umpteen number of complex circuits can be designed and fabricated using the complimentary pMOS and nMOS transistors. In a complex circuitry the signal travels through numerous transistors, at each transistor a small voltage loss may occur and the signal keeps on deteriorating. This problem is solved by the MOSFET by its feature to exhibit gain. Gain is the ability for output voltage to reach the maximum operating voltage, even if the input to the gate is slightly less than the maximum operating voltage. A first order approximation of the current through the channel is given by the equation given by Jaeger[15].

$$Id = \frac{\mu CoxW}{2L}(Vgs - Vth)^2 \qquad \text{...Equation (1)}$$

The equation shows dependence of channel current on various parameters of the MOSFET. This gives us an insight so as to which parameters should be modified to improve channel performance while still maintaining the channel ON/OFF control. Further miniaturization of the MOSFETs needs each parameter to be modified.

**2. New device Architectures**

Current mainstream production at the 130nm technology node actually produces CMOS devices with physical LG~70nm (length of FET) and 50nm devices in the 90nm technology node. The LG is expected to reach 15nm by the end of this decade and 10nm early next decade. The two crucial problems faced in scaling down silicon devices to 10nm regime are short channel control such as drain-induced-barrier-lowering (DIBL) and off-state leakage current. The off-state leakage trend should be reduced in order to limit the power dissipation in future logic devices using 10nm transistors. A fully-depleted silicon substrate is used to improve the short-channel performance such as sub threshold slope and DIBL. By adopting modified architectures like single-gate fully depleted-substrate transistor (DST), double-gate FINFET and the fully-depleted tri-gate transistor short channel performance is improved. In order to improve the total drive current for a given design space, the tri-gate devices can be connected in parallel with a common electrode as shown in Fig 2. The more silicon legs in a given design area, the higher the total drive current will be. Further improvement in the short channel performance requires gate oxide layer to be decreased than 0.8 nm. If SiO2 layer is reduced below 0.8nm it gives rise to considerable gate voltage leakage. A novel and viable solution to this hurdle is to use a material with high dielectric constant to make the gate oxide layer. This preposition is researched upon and the results show significant gate voltage leakage reduction as compared to traditional SiO2 oxide layer.

Tri-gate is fully depleted silicon substrate transistor, as shown in Fig. 2. The fabrication of the transistor is usually done on an oxide substrate, it has two gate electrodes at the sides and one at the top, the body is made out of silicon. The physical gate length ($L_G$) for all the three electrodes is generally equal as it is easier to fabricate. The physical gate width can change the side-gate transistors had a gate width of $T_{Si}$ and the top-gate transistor has physical gate width $W_{Si}$. When $L_G = W_{Si} = T_{Si}$ the tri-gate preforms delivers an optimum performance. A Tri gate CMOS with $L_G$= 60nm, $T_{Si}$= 36 nm and $W_{Si}$= 55nm has been analysed to obtain the *I-V* characteristics of the NMOS and PMOS transistors in the Tri gate as shown in the Fig. 3.

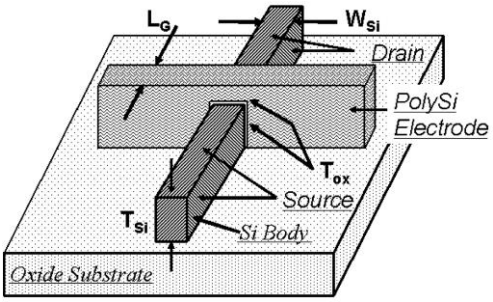


*Fig. 2. Schematic of Tri-gate transistor*

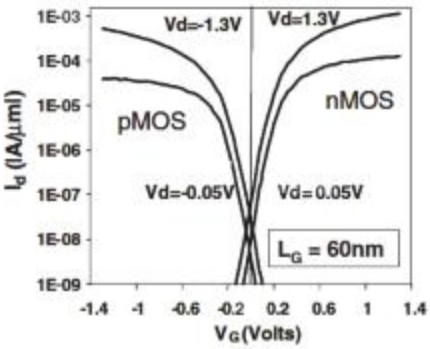


*Fig. 3. Subthreshold I-V characteristics of 60 nm Tri-gate CMOS*

It is reported that this Tri-gate CMOS has excellent short-channel performance and low values of sub threshold current. Absence of kink in the *I-V* characteristics depicts that the CMOS operated in the fully depleted region. If a higher drive current per unit design area is required, a common gate electrode with multiple Tri-gate transistors as it legs can be connected [Fig. 4]. The total drive current would be a product of the number of the legs and the drive current per leg.

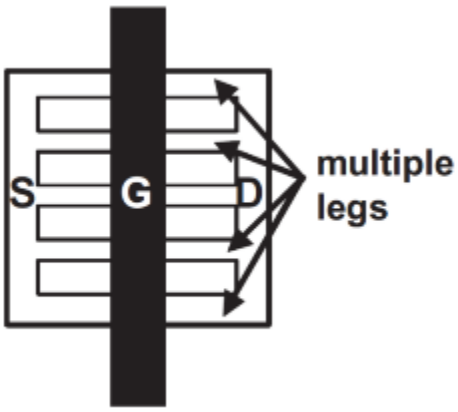


*Fig. 4. Schematic of the top view of multiple Tri-gate legs connected to a common electrode*

**3. Fabrication of CNT transistors onto CMOS circuitry**

The merits of employing CNTFETs in electrical circuits have been proved and reproduced in research labs. The major hurdle of fabrication of such CNT based circuitry at an industrial level is largescale high-precision CNT integration onto CMOS circuitry. High precision is required in placing each CNT at its desired location with appropriate density and a specified direction.To execute this task two promising approaches can be employed viz. CNT assembly by post-synthesis techniques and controlled CNT synthesis. Two of the high precision

techniques for CNT CMOS devices are Chemical assembly [1] and solution-based precise assembly like resist-assisted dielectrophoresis (DEP).[2]

A promising solution to above stated problems is to combine the scalability of capacitively coupled electrode method[3,4] and highprecision resist-assisted DEP technique[5] to devise a wafer-level CNTFET fabrication scheme. Key merits of this process are high integration density, minimized contamination, individual access and high yield[6]. Negligible hysteresis is reported when the CNTFETSs are suspended in vacuum. The duration of DEP also affects the CNT integration. After the duration of DEP is optimized more than 80% of the electrons are spanned out by a small bundle of CNTs or an individual CNT[6].

The fabrication scheme of a typical CNT lateral gate transistor by the wafer-level assembly technique is described in Materials and Methods by Cao et al[6].With little slack or tension as well as negligible resist residue, the suspended CNT channel is aligned to the desired position with Nano-precision as shown Fig. 5.To guarantee strong gate-channel coupling for CNTFET's and electromechanical coupling for CNT resonators, lateral gate has been aligned 112nm away from the CNT body as shown in Fig. 5.

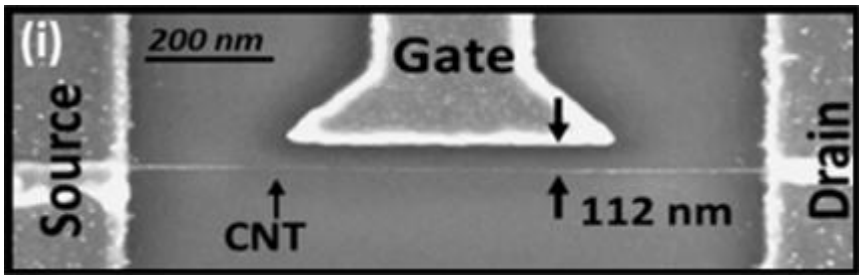


*Fig. 5. Scanning electron microscopy (SEM) of a typical CNTFET with straightened suspended CNT body showing little slack*

Studies have estimated thatit is possible to simultaneously fabricate an array consisting of 400 CNT devices in a 100 µm x 100 µmarea[6].Such an array gives high density of 3-4 million nanotube transistors per $cm^2$ which can be compared to Ultra Large Scale Integration (ULSI) of the current pre-existing technology[4]. Transfer characteristics of the suspended were studied and results indicated a very low or negligible leakage current as shown in Fig. 6, and it also suggests effective control of the CNT by the lateral gate using the 112nm air gap. The negligible hysteresis observed ensures that the transfer characteristics are not been perturbed by charge traps originating from the resist residue, the surfactant, the substrate or the water molecules on the surface of the CNT channel. The variation of width of

hysteresis for three different samples is given in Fig. 6. The reason for suppression of the hysteresis is the higher release temperature which assists in dissolving the resist and keeps CNT surface uncontaminated and prevents charge traps. To eliminate the water molecules and any absorbates on the CNT channel an annealing step is found to be effective. The above two mechanisms highly suppress the hysteresis.

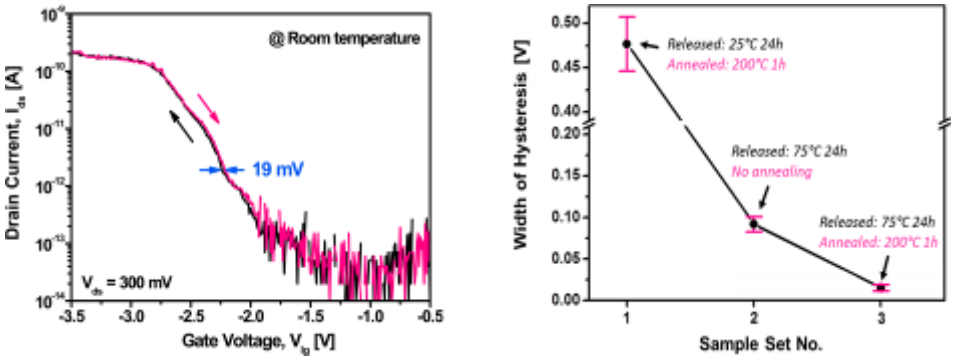


*Fig. 6. i) Transfer characteristics of the suspended CNTFET shown Fig. 5, forward and backward at sweeps at room temperature. ii) Statistical data of gate hysteresis of suspended CNTFETs at different chemical/thermal treatments under vacuum.*

The above mentioned systematic fabrication scheme has a high yield with precisely controlled location, shape of individual CNTs and their orientation. As compared to CNT adhered to the substrate, suspended CNTs offer many opportunities in displacement/chemical/optical/bio sensing[7-11] They can also be used in field of electromechanical resonance based applications such as radio frequency (RF) signal processing, mass sensing and single-device radios[12-14].Frequency tunability of CNT resonators is important for parametric amplification schemes or communication applications.

### 4. 1. Graphene based semiconductors

#### 4.1. 1. Creation of Band Gap in Graphene

Graphene shows excellent electrical, mechanical and thermal properties. Graphene by its nature can conduct current efficiently. One must be able to control the flow of current in graphene in order to exploit its superior properties and employ it in the electronics world. An excellent way of doing this is by introducing a band gap in the graphene. Several ways have been suggested to open a band gap in graphene. It can be achieved by making a graphene nano-mesh, doping graphene, confining electrons within GNR[16]. However, the creation of band gap is accompanied by lower electron mobility.

**4. 1. 2.Creation of p-n junction in Graphene**

To control current flow in graphene, one can form p-n junction diodes similar to those fabricated with silicon material. Two different approaches have pursued to create the p-n junction viz. doping via local gates, acceptor or donor impurity doping. In the first approach, the graphene is complexly patterned into sheets of nanostructures and followed by local gating of these nanostructures. Local gating is a technique in which the carrier type and density of graphene is controlled by electric field. The second approach is similar to that as done with silicon materials. A donor impurity (e.g., nitrogen) or an acceptor impurity (e.g., boron) can be used to dope graphene to make it an n-type or p-type semiconductor respectively. A promising way to produce these p-n junction in graphene is by using Direct laser Writing[17].

**4. 1. 3.Direct laser printing**

The laser-induced oxidation of 6, 13-bis (triisopropylsilylethynyl) pentacene (TIPS-pentacene) spin-cast on top of an initially p-doped graphene causes charge transfer resulting in air-stable n-doping [18]. It is been observed the Dirac point of graphene FET can be changed by altering the laser exposure time and the intensity of the laser beam. A decrease in the exposure time results in shift of the Dirac point from negative (n-type) tozero (intrinsic) and then gradually to positive (p-type) gate voltages. The advantage of this fabrication scheme is only requires a low-power visible laser system spin-coating of TIPS-pentacene.

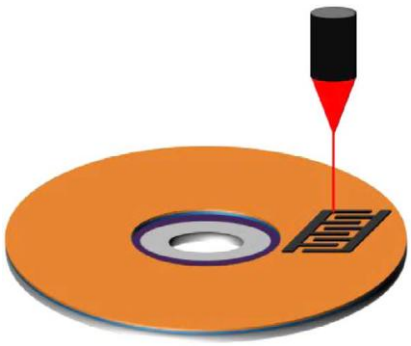

*Fig. 7. Schematic diagram showing the fabrication process for micro-supercapacitor using Lightscribe DVD burner*

This approach is very inexpensive and straight-forward is promising to succeed the throne of labour-intensive lithography[17]to produce graphene p-n junction are a large-scale. Thesimplicity of the technique even extends to using a consumergrade LightScribe DVD

burner as shown in Fig. 7. El-Kady et al[17] developed a direct fabrication scheme for patterning of on a DVD disc.[19-21] Studies have shown to produce over a 100 micro-supercapacitors in a time-frame of just 30 minutes.[20] Taking a substrate of choice which is coated with graphite oxide films, complex digital circuits can be directly patterned onto it.

**5. Flexible thin-film transistors**

Semiconducting single-wall carbon nanotubes (SWNT) which are very useful in making of flexible digital circuits, artificial skins and radio frequency devices due to its exceptional electrical properties and intrinsic mechanical strength.[22] Single-wall carbon nanotubes (SWNTs) are perfect solution for channel material of thin-film transistors (TFTs) for flexible macroelectronics,[23-24] displays, and sensors.[25-26]Carbon nanotubes have great mechanical flexibility compared to traditional channel materials like amorphous silicon and polysilicon. Apart from the phenomenal intrinsic electrical properties of semiconducting SWNTs, they exhibit considerable advantages over organic materials for TFTs such as mobility on-off ratio, and stability against moisture and oxygen.[27-28] . Therefore, rigorous research efforts have been in progress to flexible SWNT TFTs for its applications in digital circuits, active-matrix-based displays, and sensors.[29-31]

**6. Semiconducting Nanowires (S-NW)**

S-NWs are long thin wires made up of semiconducting materials, such as silicon or germanium which are fabricated with diameter as small as 3nm[32-33] and have a length of a few hundreds of micrometres[34]. S-NWs can be used as interconnect wires to carry signals as well as be used as an active device. On the contrary an individual CNT is either an active device or a wire, a single S-NW can be both an active device and can also connect two digital devices. In large electronic circuits there are enormous number of wires which connect all the transistors, capacitors and other device. These wires may overlap and may exist in very close proximity to other wires. In current Very Large Scale Integration (VLSI) and large circuits, majorly copper wires are used. Significant research has been done in replacing these copper wires with nanowires of a semiconducting nature.

**6.1 Fabrication of p-n junction S-NW**

Semiconducting Nanowires (S-NW) made of silicon and germanium with a very high aspect ratio and diameters within range of 3nm have been fabricated as shown in Fig. 9. These nanowires are fabricated using Chemical vapour deposition (CVD) process on a gold droplet.

When GaP vapours are passed the gold acts as a catalyst and the GaP starts accumulating below the surface of the gold droplet. Another gas say (GaN) can be passed and this GaN layer starts accumulating on top of pre-existing GaP layer with gold droplet as a head. Using this technique we can fabricate p-doped and n-doped stretches of nanowires thus creating a p-n junction transistor at nano scale.

**6.2 Fabrication of FETs with S-NW**

A field effect transistor (FET)[Fig. 8] can be created if a nanowire has a small section that contains fewer carriers than the rest of the wire[35]. Lowering the concentration of the atoms that are doped in the growing atmosphere for a period of time can make this lesser-doped region. A FET is created whensome other wire is arranged over the top most part of this region, with an insulator to separate the two wires, also a charge is place on the top wire in order to control the current and to deplete the carriers in the FET regions of the lower wires [36].

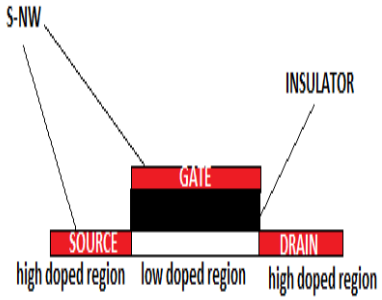


*Fig. 8. S-NW based FET*

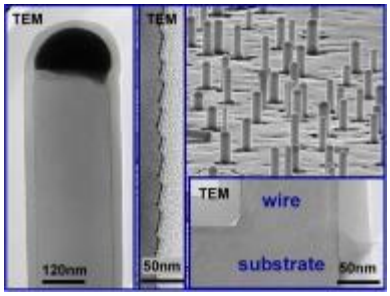


*Fig. 9.TEM of Si NWs grown by EBE. The dark gold top & Si NWs are visible*

Application of S-NW in circuit poses certain challenges. S-NW is very sensitive to particles suspended in the atmosphere. They get easily contaminated or oxidized. The S-NW used may be single walled which means they offer 1-D conductance, a single defect in one of the atoms of the wire leads to perturbation in the flow of current across the whole wire. Hence defect free fabrication of S-NW is a major criterion which will determine its application in electronic circuits.

## CONCLUSION

The invention of the transistor in 1947 is one of the most important inventions of the 20th century. It is essentially the fundamental building block of electrical, digital circuits. The size of digital circuits has kept on reducing and is governed by the famous Moore's law. The time

has dawned upon us where the limitations to further miniaturization of the CMOS circuits have come into light. Nano-electronics shows promise to continue the miniaturization of Integrated Circuits(IC). Modification of the pre-existing structure of the MOSFETs into depleted tri-gate transistors seems to be promising approach to enable miniaturization. Nano-materials like CNT, SWCNT, SNW and graphene show superior electrical & physical properties as compared to silicon. CNTFETs have great potential in high-performance and energy-efficient digital electronics. Band gap has been created in graphene; p-n junctions have been created using Direct Laser printing technique and it opens door to cheap, facile large scale fabrication of graphene electronics. The method of CVD is been used to fabricate p-n junction diodes in a single S-NW, a combination of S-NWs have been employed to create FET. Aforementioned technologies are still in research labs. To meet the electronic demand of the world, billions of circuits of circuits are to be manufactured every day. Fabrication of these nano-devices without any defects and high precision is a major obstacle in the commercialization of this technology. It is of paramount importance to model and employ robust, cheap and facile fabrication processes to enable large scale production of these advanced technologies. Control over fabrication and manipulation these materials along with precise placement on circuit boards will empower us to create highly dense integrated circuits which shall be faster, more robust and will pave the way to the era of Nanoelectronics.

## REFERENCES AND NOTES

1. Park, Hongsik, et al. "High-density integration of carbon nanotubes via chemical self-assembly." *Nature nanotechnology* 7.12 (2012): 787-791.
2. Cao, J.; Nyffeler, C.; Lister, K.; Ionescu, A. M. Resist-Assisted Assembly of Single-Walled Carbon Nanotube Devices with Nanoscale Precision. Carbon 2012, 50, 1720–1726.
3. Krupke, R., et al. "Simultaneous deposition of metallic bundles of single-walled carbon nanotubes using ac-dielectrophoresis." *Nano Letters* 3.8 (2003): 1019-1023.
4. Vijayaraghavan, Aravind, et al. "Ultra-large-scale directed assembly of single-walled carbon nanotube devices." *Nano letters* 7.6 (2007): 1556-1560.
5. Sazonova, V. A Tunable Carbon Nanotube Resonator. Ph.D. Thesis, Cornell University, Ithaca, NY, 2006.

6. Cao, Ji, Sebastian T. Bartsch, and Adrian M. Ionescu. "Wafer-Level Hysteresis-Free Resonant Carbon Nanotube Transistors." *ACS nano* 9.3 (2015): 2836-2842.
7. Franklin, Nathan R., et al. "Integration of suspended carbon nanotube arrays into electronic devices and electromechanical systems." *Applied Physics Letters* 81.5 (2002): 913-915.
8. I Ionescu, Adrian M., et al. "Ultra low power: Emerging devices and their benefits for integrated circuits." *Electron Devices Meeting (IEDM), 2011 IEEE International*. IEEE, 2011.
9. Helbling, Thomas, et al. "Suspended and non-suspended carbon nanotube transistors for NO2 sensing–A qualitative comparison." *physica status solidi (b)* 245.10 (2008): 2326-2330.
10. Mann, David, et al. "Electrically driven thermal light emission from individual single-walled carbon nanotubes." *Nature nanotechnology* 2.1 (2007): 33-38.
11. Stampfer, C., et al. "Nano-electromechanical displacement sensing based on single-walled carbon nanotubes." *Nano letters* 6.7 (2006): 1449-1453.
12. Jensen, K., Kwanpyo Kim, and A. Zettl. "An atomic-resolution nanomechanical mass sensor." *Nature nanotechnology* 3.9 (2008): 533-537.
13. Sazonova, Vera, et al. "A tunable carbon nanotube electromechanical oscillator." *Nature* 431.7006 (2004): 284-287.
14. Rutherglen, Chris, and Peter Burke. "Carbon nanotube radio." *Nano Letters*7.11 (2007): 3296-3299.
15. R.C. Jaeger, *Microelectronic Circuit Design*, Boston, MA, WCB/McGraw-Hill, 1997.
16. Novoselov, Konstantin S., et al. "A roadmap for graphene." *Nature* 490.7419 (2012): 192-200.
17. El-Kady, Maher F., and Richard B. Kaner. "Direct laser writing of graphene electronics." *ACS nano* 8.9 (2014): 8725-8729.
18. Seo, Byung Hwa, Jongmin Youn, and Moonsub Shim. "Direct Laser Writing of Air-Stable p–n Junctions in Graphene." *ACS nano* 8.9 (2014): 8831-8836.
19. El-Kady, Maher F., et al. "Laser scribing of high-performance and flexible graphene-based electrochemical capacitors." *Science* 335.6074 (2012): 1326-1330.

20. El-Kady, Maher F., and Richard B. Kaner. "Scalable fabrication of high-power graphene micro-supercapacitors for flexible and on-chip energy storage."*Nature communications* 4 (2013): 1475.
21. Strong, Veronica, et al. "Patterning and electronic tuning of laser scribed graphene for flexible all-carbon devices." *ACS nano* 6.2 (2012): 1395-1403.
22. Cao, Xuan, Yu Cao, and Chongwu Zhou. "Imperceptible and Ultraflexible p-Type Transistors and Macroelectronics Based on Carbon Nanotubes." *ACS nano* (2015).
23. Sun, D. M.; Timmermans, M. Y.; Tian, Y.; Nasibulin, A. G.; Kauppinen, E. I.; Kishimoto, S.; Mizutani, T.; Ohno, Y. Flexible HighPerformance Carbon Nanotube Integrated Circuits. Nat. Nanotechnol. 2011, 6, 156−161.
24. Park, S.; Vosguerichian, M.; Bao, Z. A Review of Fabrication and Applications of Carbon Nanotube Film-Based Flexible Electronics. Nanoscale 2013, 5, 1727−1752
25. Yeom, C.; Chen, K.; Kiriya, D.; Yu, Z.; Cho, G.; Javey, A. LargeArea Compliant Tactile Sensors Using Printed Carbon Nanotube Active-Matrix Backplanes. Adv. Mater. 2015, 27, 1561−1566.
26. Zhang, J.; Wang, C.; Zhou, C. Rigid/Flexible Transparent Electronics Based on Separated Carbon Nanotube Thin-Film Transistors and Their Application in Display Electronics. ACS Nano 2012, 6, 7412−7419.
27. Sekitani, T.; Zschieschang, U.; Klauk, H.; Someya, T. Flexible Organic Transistors and Circuits with Extreme Bending Stability. Nat. Mater. 2010, 9, 1015−1022.
28. Wang, C.; Takei, K.; Takahashi, T.; Javey, A. Carbon Nanotube Electronics–Moving Forward. Chem. Soc. Rev. 2013, 42, 2592−2609.
29. Sun, D. M.; Timmermans, M. Y.; Kaskela, A.; Nasibulin, A. G.; Kishimoto, S.; Mizutani, T.; Kauppinen, E. I.; Ohno, Y. Mouldable AllCarbon Integrated Circuits. Nat. Commun. 2013, 4, 2302−2309.
30. Lau, P. H.; Takei, K.; Wang, C.; Ju, Y.; Kim, J.; Yu, Z.; Takahashi, T.; Cho, G.; Javey, A. Fully Printed, High Performance Carbon Nanotube Thin-Film Transistors on Flexible Substrates. Nano Lett. 2013, 13, 3864−3869.
31. Kim, B.; Jang, S.; Geier, M. L.; Prabhumirashi, P. L.; Hersam, M. C.; Dodabalapur, A. High-Speed, Inkjet-Printed Carbon Nanotube/ Zinc Tin Oxide Hybrid Complementary Ring Oscillators. Nano Lett. 2014, 14, 3683−3687.

32. Cui, Yi, et al. "Diameter-controlled synthesis of single-crystal silicon nanowires." *Applied Physics Letters* 78.15 (2001): 2214-2216.
33. Morales, Alfredo M., and Charles M. Lieber. "A laser ablation method for the synthesis of crystalline semiconductor nanowires." *Science* 279.5348 (1998): 208-211.
34. Y. Wu, P. Yang, "Germanium Nanowire Growth via Simple Vapor Transport," Chemistry of Materials, vol. 12, 2000, pp.605-607.
35. M. Gudiksen et al., "Growth of Nanowire Superlattice Structures for Nanoscale Photonics and Electronics," Letters to Nature, vol. 415, no. 6872, 2002, pp. 617-620.
36. Y. Huang et al., "Logic Gates and Computation from Assembled Nanowire Building Blocks," Science, vol. 294, no. 5545, 2001, pp. 1313-1316.
37. Giovannetti, G. A. K. P. A., et al. "Doping graphene with metal contacts." *Physical Review Letters* 101.2 (2008): 026803.
38. Gierz, Isabella, et al. "Atomic hole doping of graphene." *Nano letters* 8.12 (2008): 4603-4607.
39. Varykhalov, A., et al. "Effect of noble-metal contacts on doping and band gap of graphene." *Physical Review B* 82.12 (2010): 121101.
40. Song, Seung Min, et al. "Determination of work function of graphene under a metal electrode and its role in contact resistance." *Nano letters* 12.8 (2012): 3887-3892.
41. Nouchi, Ryo, and Katsumi Tanigaki. "Charge-density depinning at metal contacts of graphene field-effect transistors." *Applied Physics Letters* 96.25 (2010): 253503.
42. Xia, Fengnian, et al. "The origins and limits of metal-graphene junction resistance." *Nature nanotechnology* 6.3 (2011): 179-184.
43. Grosse, Kyle L., et al. "Nanoscale Joule heating, Peltier cooling and current crowding at graphene-metal contacts." *Nature nanotechnology* 6.5 (2011): 287-290.
44. Li, Xuesong, et al. "Large-area synthesis of high-quality and uniform graphene films on copper foils." *Science* 324.5932 (2009): 1312-1314.
45. Das, Anindya, et al. "Monitoring dopants by Raman scattering in an electrochemically top-gated graphene transistor." *Nature nanotechnology* 3.4 (2008): 210-215.